Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A probe assemblage for providing electrical connection simultaneously between one or more integrated circuits on a semiconductor wafer and a circuit test equipment, said assemblage including:

an interposer comprising a dielectric material having two major surfaces,

a plurality of protruding contact elements on one major surface of said interposer, each element corresponding to a test pad on one or more integrated circuits,

a plurality of conductive vias connecting each of said contact elements to a metallized pad on the second surface of said interposer,

a plurality of conductive leads fanning outward from said metallized pads to a standardized array of interposer connectors,

a compliant material underlying said contact elements on the first surface, and/or said interposer connectors on the second surface of the interposer,

a probe card having an array of connectors corresponding to said interposer connector array, and

means for attaching said probe card to said interposer.

2. (original) An assemblage as in claim 1 wherein said protruding contact elements comprise a noble or oxide limiting metal.

3. (original) An assemblage as in claim 1 wherein said protruding contact elements are stud bumps.

4. (original) An assemblage as in claim 1 wherein said contact elements are microwires.

5. (original) An assemblage as in claim 1 wherein the interposer has a coefficient of thermal expansion in the range of 2 to 10 PPM.

6. (original) An assemblage as in claim 1 wherein said interposer includes one or more buried metal ground planes.

7. (currently amended) An assemblage as in claim 1 wherein said pads and [[connecting]] conductive leads on the interposer comprise a first layer of copper and second layer of a laser ablatable material.

8. (currently amended) An assemblage as in claim 1 wherein said pads and [[connecting]] conductive leads on the interposer are patterned by laser ablation in combination with chemical etching.

9. (currently amended) An assemblage as in claim 1 wherein the [[conductor]] pattern [[of]] for the conductive leads and pads is software generated and input to a laser.

10. (currently amended) An assemblage as in claim 1 wherein said chip contact elements are spaced more closely than the probe card connectors.

11. (original) An assemblage as in claim 1 wherein said connectors on the second surface of the interposer mate to an array of connectors on a probe card.

12. (original) An assemblage as in claim 1 wherein said connectors on the probe card are arrayed in a universal pattern common to multiple circuit devices.

13. (original) An assemblage as in claim 1 wherein said means to attach the interposer to the probe card is a plurality of threaded machine screws.

14-19. (canceled)

20. (original) A method of forming an assemblage for simultaneously providing electrical connection between one or more integrated circuits on a semiconductor wafer and a circuit tester, including the following steps:

-providing an dielectric interposer having thermal expansion characteristics similar to that of silicon, and having a plurality of conductive vias at locations corresponding to the

distance between chip contact pads which extending from the first major surface to the second major surface of the interposer,

-affixing a layer of highly conductive metal on each major surface,

-patterning an array of pads corresponding to chip contact pads on the first surface,

- patterning an array of pads at the via egress point on the second surface and an array of conductive leads terminating in a standardized pattern,

- bonding a chip contact element to each patterned contact pad on the first surface, and a connector element on the terminal of each lead on the second surface,

- providing a compliant material layer underlying the chip contact elements, and/or probe connector on the interposer,

- providing a probe card having a mating connector to that on said interposer, and

- aligning said connectors, and mechanically attaching.

21. (original) A method as in claim 20 wherein said patterns on the interposer surface are generated by using a software [[input to]] and a computer controlled laser.

22. (original) A method as in claim 20 wherein said metal patterns are formed by at least partially by laser ablation.

23. (original) A method as in claim 20 wherein said metal patterns are formed by photolithography and chemical etching.